25.3 A 4.7mW 0.32mm² 10b 30MS/s Pipelined ADC Without a Front-End S/H in 90nm CMOS

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Low-power small-area ADCs with 10b resolution and several tens of MHz sampling rate are considered to be one of the significant components in battery-operated commercial applications including data communication and image signal-processing systems. In these applications, the pipelined architecture with a front-end S/H has been widely used for processing a wide-bandwidth input signal with a high accuracy. Holding an analog input signal, the S/H reduces the aperture error, defined as $V_e=2\pi \cdot f_{in} \cdot V_{REF}(\Delta \cdot \tau)$, between the first-stage multiplying DAC (MDAC) and the first-stage flash ADC. The S/H, however, not only consumes a large portion of the ADC overall power consumption to drive the next MDAC with high accuracy but also adds noise and distortion to the input signal. Conventional design techniques without using the S/H have several disadvantages; a preamp in the first-stage flash ADC requires 2 capacitors to sample analog input and reference voltages, and the first-stage MDAC consumes a large amount of power to retain the same conversion speed [1].

Figure 25.3.1 shows the proposed 10b 30MS/s pipelined ADC operating from a 1.0V supply. The ADC consists of 3 MDACs, 4 flash ADCs, a digital correction logic (DCL) block, a BGR, a reference, and a clock generator. In this architecture, the elimination of the S/H scheme is employed with little modification of the conventional MDAC and preamp circuits. For further power and area reduction, the ADC adopts an opamp-sharing technique between MDAC2 and MDAC3, and a resistor-ladder sharing technique between F2 and F3 [2]. The BGR for reference and bias voltages of the ADC use a 3.3V supply. The CK signal, 2× the frequency of the ADC operation clock, is divided by 2, through a D-FF, to generate non-overlap clocks Q1 and Q2. The additional clocks, QS and QL, are obtained by a combination of CK and Q2.

The front-end stage of the proposed ADC, as shown in Fig. 25.3.2, is similar to that of the conventional ADC except for the S/H stage. The 3b MDAC1 uses a reversed-nested Miller compensation (RNMC) 3-stage opamp in order to obtain a high DC gain and a large output swing using a 1.0V supply [3]. The 3b flash ADC1, composed of 8 preamps using a single capacitor and latches, generates a thermometer digital code for the residue amplification of the MDAC1. The bootstrapping technique is not applied to all sampling switches to save area. Figure 25.3.3 shows the detailed timing diagrams of the front-end stage. In the conventional front-end stage with the S/H, the preamps typically sample the reference voltages first while the S/H samples the analog input signal during Q1 phase. In the hold-phase Q2 of the S/H, the preamps amplify the difference of the reference and the S/H output, and the MDAC1 samples the S/H output. The thermometer code generated by latches is transferred to the MDAC1 at falling edge of Q2P. On the other hand, in the proposed front-end stage without the S/H, both the sampling and amplifying of the preamps are performed in Q2 phase. During QS phase, the analog input signal is directly sampled on capacitors CM1 to CM8 of the MDAC1 and capacitors CF1 to CF8 of the preamps by the same clock QSP. During QL phase, the reference voltages REF1 to REF8 are connected to the capacitors CF1 to CF8 and the preamps amplify the difference of the sampled analog input and the reference voltages. At the same time, all switches of the MDAC1 are turned off and the sampled charge in the capacitors CM1 to CM8 is held. Next, the thermometer code is transferred to the MDAC1 at the falling edge of Q2P like the conventional front-end stage with the S/H. Since the MDAC1 and the preamps simultaneously sample the input signal at the falling edge of QSP, the aperture error is greatly reduced. Also, the sampling switches and capacitors of the MDAC1 and the preamps are designed to have a similar RC time constant to minimize the signal delay mismatch in each signal path. Therefore, the proposed scheme is implemented with little modification of the conventional preamp and MDAC1 circuits using the additional clocks QS and QL, and does not need the large power consumption of the MDAC1 because of the identical amplification period.

Although the proposed scheme is efficient in terms of aperture error reduction, implementation and area, the QS and QL that have half-high duration of Q2 shorten the sampling time of the analog input and the amplification period of the preamp. The shorter sampling time is solved by increasing the size of the sampling switches and hence, reducing the RC time constant and improving the switch linearity. Also the preamp with open-loop architecture does not impose any speed limitation on the pipelined ADC. The power consumption of the high-speed preamp stays comparable to that of the conventional preamp by using power-save mode that does not supply current to the preamp completely during Q1 phase. In this scheme, the power-save mode does not affect the operation of the preamp during QL phase due to the sufficient start-up time corresponding to QS.

The pipelined ADC is fabricated in a 90nm CMOS process as shown in Fig. 25.3.4. The active die area of the ADC is $0.32mm^2$(=0.62mm×0.52mm) with the BGR. The measured DNL and INL at 10b accuracy are shown in Fig. 25.3.5. The DNL is +0.47/-0.44LSB and the INL is +0.65/-0.80LSB. Figure 25.3.6(a) and Fig. 25.3.6(b) show the measured FFT plot and dynamic performance versus sampling frequency of the ADC with the external input band-pass filter to reduce the noise from the signal source. The measured SNDR, SFDR, and ENOB are 58.4dB, 75.2dB, and 9.4b at a 2MHz input and a 30MHz sampling frequency, respectively. In the measured dynamic-performance versus sampling-frequency plot for a 2MHz input frequency, the prototype ADC maintains the SNDR better than 58dB up to 35MS/s. Figure 25.3.6(c) shows the dynamic performance versus input frequency at a 30MHz sampling frequency without the external-input band-pass filter. If the analog input signal passing through the band-pass filter is applied to the ADC, the SNDR is expected to maintain ~55dB up to 14.8MHz input frequency. The ADC dissipates about 4.7mW when operating at 30MS/s from a 1.0V supply excluding the BGR for 3.3V. The FOM, defined as $Power/(2^{ENOB} \cdot f_s)$, is 0.23pJ/conversion-step at a 2MHz input with 30MS/s. The measured performance of the prototype ADC is summarized in Fig. 25.3.7.

References:

[1] D. Y. Chang, "Design Techniques for a Pipelined ADC Without Using a Front-End Sample-and-Hold Amplifier," *IEEE Trans. Circuits Syst.I*, vol.51, pp. 2123-2132, Nov., 2004.

[2] Y. D. Jeon, S.-C. Lee, K.-D. Kim, et al., "A 5-mW 0.26-mm² 10-bit 20-MS/s Pipelined CMOS ADC with Multi-Stage Amplifier Sharing Technique," *Proc. ESSCIRC,* pp. 544-547, Sept., 2006.

[3] K. P. Ho, C.F. Chan, C.S. Choy, et al., "Reversed Nested Miller Compensation with Voltage Buffer and Nulling Resistor," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1735-1738, Oct., 2003.

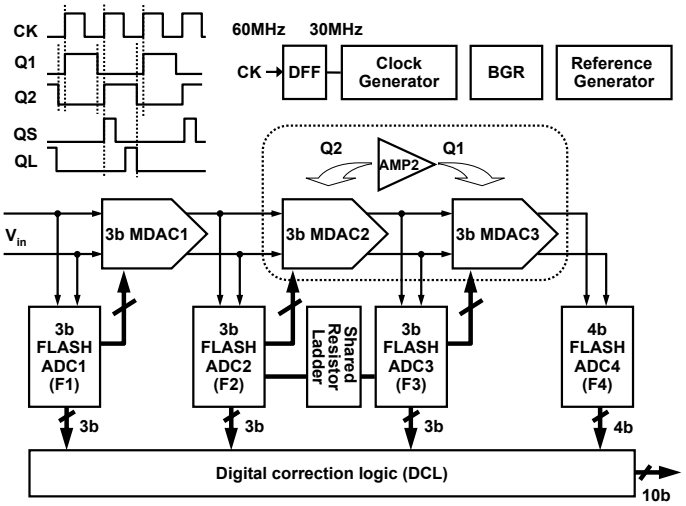

Figure 25.3.1: Architecture of the proposed 10b 30MS/s pipelined ADC.

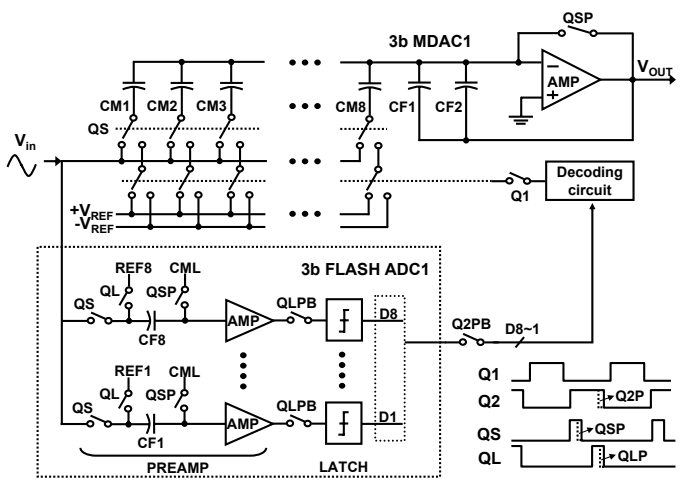

Figure 25.3.2: Front-end stage of the proposed ADC.

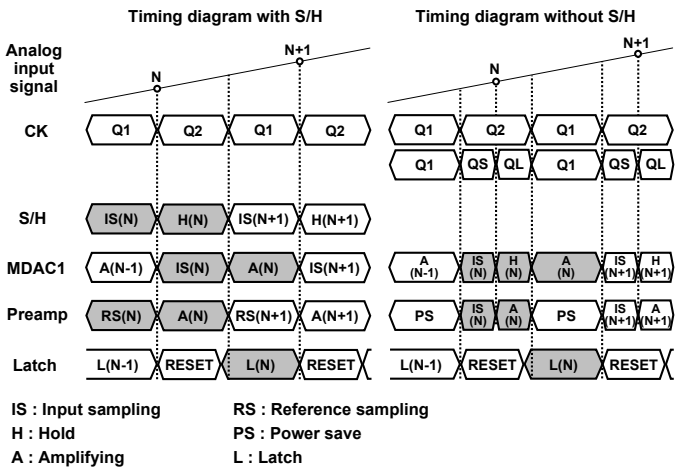

Figure 25.3.3: Timing diagrams of the front-end circuits.

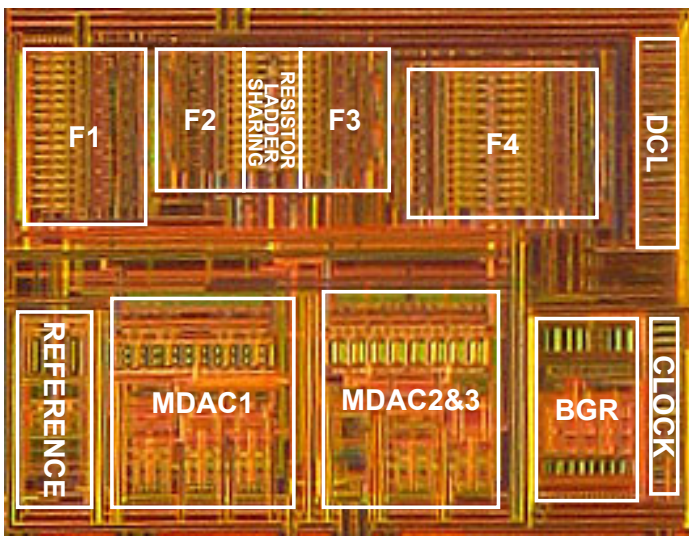

Figure 25.3.4: Die micrograph.

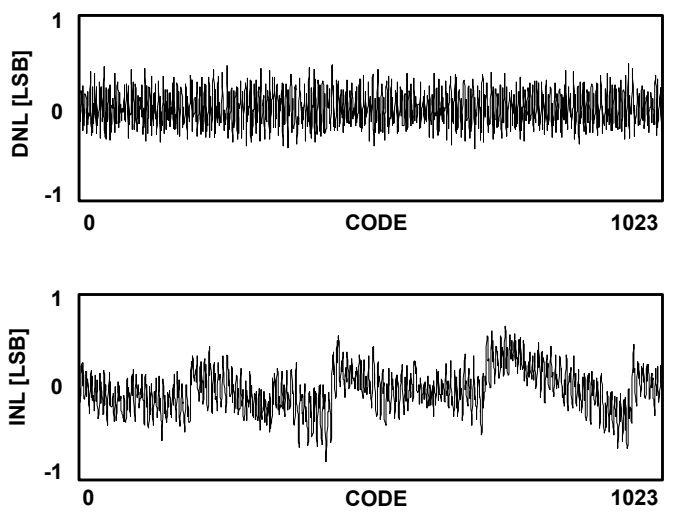

Figure 25.3.5: Measured DNL and INL.

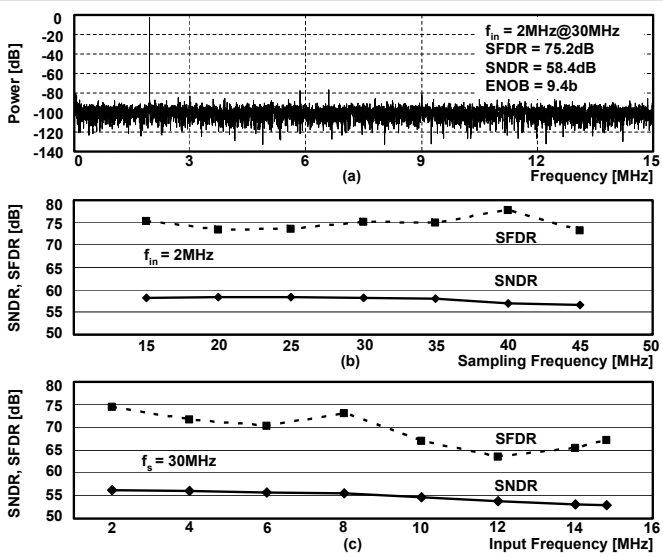

Figure 25.3.6: Measured FFT plot and dynamic performances.

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Process	90nm 1P6M CMOS
Resolution	10b
Conversion Rate	30MS/s
Supply Voltage	1.0V
Input Range	$1.0V_{pp}$
DNL, INL	+0.47/-0.44LSB, +0.65/-0.80LSB
SNDR	58.4dB @ f_{in}=2MHz
SFDR	75.2dB @ f_{in}=2MHz
Power Consumption	4.7mW
FOM	0.23pJ/conversion-step
Active Area	$0.32mm^2$ (= $0.62x0.52mm^2$)

Figure 25.3.7: Performance summary.

